

Hardware-Efficient Optical Communication Architectures for AI Data Center Networks

Chloe A. Clay

Department of Computer Science, George Mason University, Fairfax, VA, USA.
chloework@gmu.edu

Vivianne Soderlund

Department of Computer Science, Binghamton University, Binghamton, NY, USA.
vivianne@binghamton.edu

Gitte Mulichen

Department of Electrical Engineering and Computer Science, University of Missouri,
Columbia, MO, USA.
gittem@missouri.edu

Abstract

Artificial intelligence data centers are increasingly constrained by the electrical interconnect fabric that links accelerators, memory, storage, and switching resources. Large-scale training and inference workloads generate intense east-west traffic, synchronization-heavy communication patterns, and bursty demand that traditional electrical packet switching handles with growing difficulty in terms of bandwidth density, reach, latency, and energy. Optical communication architectures offer a promising path toward higher throughput and lower signaling loss, but they are not automatically efficient. Hardware efficiency depends on the co-design of photonic devices, packaging, switching, control planes, thermal management, and deployment governance. This paper examines hardware-efficient optical communication architectures for AI data center networks from a system-level perspective. It analyzes the requirements imposed by distributed AI workloads, reviews silicon photonic and wavelength-division multiplexing building blocks, and compares point-to-point, circuit-switched, packet-switched, and hybrid electrical-optical architectures. The discussion emphasizes structural trade-offs among bandwidth, latency, energy, cost, reliability, and sustainability. It also considers operational governance, supply-chain resilience, fairness in access to advanced computing infrastructure, and policy implications. The paper argues that hardware-efficient optical AI fabrics require not only improved transceivers and switches but also coherent control, telemetry, standardization, and lifecycle accountability. Frequency-referenced multiplexing and related low-latency bandwidth-guaranteed approaches illustrate how physical-layer innovation can reshape network-level guarantees, yet their benefits depend on holistic architecture and governance choices. The conclusion outlines a research agenda for co-designed, sustainable, and equitable optical AI infrastructure.

Keywords

optical interconnects; AI data centers; silicon photonics; wavelength-division multiplexing; hardware efficiency; network architecture; sustainability; governance.

1. Introduction

The rapid expansion of artificial intelligence has transformed data centers from general-purpose computing facilities into specialized systems optimized for dense matrix computation, high-bandwidth memory access, and collective communication. Training large models requires thousands of accelerators to exchange gradients, parameters, activations, and optimizer states across tightly coupled domains. Inference at scale introduces additional constraints involving request fan-out, low-latency response, and cost-sensitive utilization. These workloads place unprecedented pressure on the network fabric, which must deliver high bandwidth with predictable latency while consuming a diminishing share of total facility power. Electrical interconnects, although mature and widely deployed, face fundamental limits in reach, bandwidth density, and energy per bit as signaling rates increase. This has motivated sustained interest in optical communication architectures that use light to carry data between chips, boards, racks, and rows [1], [2], [3].

Optical interconnects are attractive because they can support longer reach with lower loss, provide wavelength parallelism, and reduce the need for bulky copper cabling and equalization. However, the transition from electrical to optical fabrics is not a simple substitution. Photonic devices require lasers, modulators, photodetectors, waveguides, multiplexers, and packaging that introduce new failure modes, thermal sensitivities, and manufacturing constraints. Switching in the optical domain may reduce energy per bit but can increase reconfiguration latency or control complexity. Co-packaged optics can improve bandwidth density but complicates serviceability and thermal design. Therefore, the central question is not whether optics can be used in AI data centers, but which optical architectures are hardware-efficient under realistic workload, cost, reliability, and sustainability constraints.

This paper adopts a system-level perspective on hardware-efficient optical communication architectures for AI data center networks. It treats hardware efficiency as a multidimensional property encompassing delivered bandwidth per watt, latency under load, cost per port, reliability, maintainability, and embodied resource use. The analysis proceeds through the requirements of AI workloads, the capabilities and limitations of optical building blocks, architectural alternatives, trade-off analysis, governance, sustainability, and future research directions. The paper also examines how physical-layer innovations such as frequency-referenced multiplexing can alter network-level guarantees, while cautioning that such gains are realized only when integrated with scheduling, telemetry, and policy frameworks.

2. AI Data Center Network Requirements and Constraints

AI data center networks differ from conventional cloud networks because their dominant traffic patterns are often synchronized, predictable in structure but bursty in intensity, and highly sensitive to tail latency. Distributed training frequently relies on collective operations such as all-reduce, all-gather, and reduce-scatter. These operations create phases in which many accelerators communicate simultaneously, followed by computation phases. The network must therefore handle incast, multicast-like dissemination, and rapid reconfiguration without starving other tenants. Inference workloads, by contrast, may involve smaller messages, strict response-time targets, and heterogeneous service-level agreements. A single fabric must often support both patterns, which complicates static overprovisioning and favors architectures with dynamic resource allocation [1], [4].

Electrical packet switching has scaled impressively through higher SerDes rates, larger switch radices, and advanced modulation. Nevertheless, the energy required to move bits over copper rises sharply with distance and data rate. High-speed electrical links require equalization, forward error correction, and retiming, all of which consume power and add latency. Thermal

density near switch ASICs and accelerator packages further constrains feasible port counts. As rack power budgets tighten, the network's share of facility energy becomes a first-order design concern rather than a secondary optimization. Optical links can alleviate some of these pressures by providing lower-loss transmission and wavelength parallelism, but they introduce electro-optical conversion, laser bias control, and photonic packaging overhead [5], [6], [7].

The constraints on AI networks are therefore simultaneously technical, economic, and operational. Technically, the fabric must deliver high bandwidth density, low latency, low jitter, and graceful degradation under failure. Economically, it must justify capital and operational expenditure against rapidly changing accelerator generations. Operationally, it must be deployable, diagnosable, and repairable by data center teams with finite training and spares. These constraints mean that hardware efficiency cannot be measured solely by transceiver energy per bit. It must also account for switch utilization, cabling complexity, cooling load, failure recovery time, and the embodied carbon of photonic components. A network that saves signaling energy but requires excessive cooling or frequent laser replacement may be less efficient in practice [2], [4], [6].

3. Optical Communication Building Blocks and Hardware Efficiency

Hardware-efficient optical architectures build on a photonic stack that includes light sources, modulators, waveguides, multiplexers, photodetectors, and electronic drivers. Silicon photonics has emerged as a central platform because it allows many optical components to be fabricated with complementary metal-oxide-semiconductor processes, potentially enabling low-cost integration and high volume. Modulators based on carrier depletion or accumulation can encode data at high rates, while germanium photodetectors provide on-chip reception. Waveguides and grating couplers route and couple light, and arrayed waveguide gratings or microring resonators perform wavelength multiplexing and demultiplexing. Each component contributes to insertion loss, power consumption, thermal drift, and yield, so component-level efficiency must be evaluated within the full link budget [8], [9], [15].

Wavelength-division multiplexing is especially important for AI fabrics because it allows multiple data streams to share a single fiber or waveguide, increasing bandwidth density without proportionally increasing cable count. Coarse and dense wavelength-division multiplexing can support parallel lanes, but laser wavelength stability and thermal control remain challenging. Frequency-referenced multiplexing, as demonstrated in recent work, offers a way to provide guaranteed bandwidth and low latency by referencing many optical carriers to a common frequency comb or reference. This approach can reduce frequency drift, simplify tuning, and support deterministic latency, which is valuable for synchronized AI communication. However, its system-level benefits depend on the availability of compatible transceivers, switching elements, and control algorithms that can exploit stable frequency grids [13]. The required reference thus illustrates a broader principle: physical-layer stability can translate into network-level predictability, but only when the architecture can use that stability effectively.

Integration strategy is another determinant of hardware efficiency. Discrete optical components offer flexibility but increase size, loss, and assembly cost. Hybrid integration combines separately fabricated photonic and electronic chips, often using flip-chip bonding or interposers. Monolithic integration places photonic and electronic functions on the same die or wafer, reducing parasitics and improving energy efficiency but imposing complex process constraints. Co-packaged optics moves optical engines close to switch ASICs, shortening

electrical traces and reducing high-speed electrical signaling power. Yet co-packaging complicates thermal management, testability, and replacement. Pluggable optics, in contrast, preserve serviceability but consume more power and front-panel density. The trade-off between integration and serviceability is central to AI data center design because accelerator generations change quickly and operators require repairable infrastructure [10], [14], [16], [17].

Hardware efficiency also depends on the optical switch or fabric element. Optical circuit switches can reconfigure entire wavelength paths with low per-bit energy, but they may require milliseconds to reconfigure and are poorly suited to fine-grained packet bursts. Optical packet switches can react quickly but often need buffering, synchronization, or fast tunable lasers that increase complexity. Hybrid approaches combine electrical packet switching for fine-grained traffic with optical circuit switching for large elephant flows. The practical efficiency of such hybrids depends on traffic classification, flow detection, and scheduling overhead. If the control plane cannot identify and route large flows quickly, the optical path may remain underutilized while electrical switches absorb the load. Therefore, hardware efficiency is inseparable from software and control co-design [10], [11], [12].

4. Architectural Options for Optical AI Data Center Networks

Several architectural families have been proposed for optical AI data center networks. Point-to-point optical links replace copper for rack-to-rack or row-to-row connections. They are conceptually simple and can improve reach and bandwidth density, but they do not by themselves change switching topology. Optical circuit-switched fabrics establish end-to-end light paths through mirrors, microelectromechanical systems, or wavelength-selective switches. These fabrics can provide high throughput and low energy per bit for sustained flows, and they can be reconfigured to match changing traffic matrices. Their weakness is latency and granularity: circuit setup and tear-down may be slow relative to packet-level bursts, and the fabric may waste capacity when flows are short or highly dynamic [10], [12].

Optical packet-switched fabrics aim to combine optical bandwidth with packet-level flexibility. They may use fast tunable lasers, optical buffers, or wavelength converters. In practice, optical buffering is difficult because light cannot be stored compactly without conversion to the electrical domain or long fiber delays. Synchronization and contention resolution add overhead. As a result, pure optical packet switching has not displaced electrical packet switching in general-purpose data centers. For AI workloads, however, the traffic structure may be more favorable because collective operations generate large, synchronized transfers. If the control plane can predict these phases, it can schedule optical circuits or wavelength paths in advance, reducing the need for packet-level optical switching. This suggests a workload-aware architecture in which AI schedulers expose communication phases to the network controller [11], [12].

Hybrid electrical-optical architectures are currently the most plausible near-term path. In such designs, electrical switches handle latency-sensitive and fine-grained traffic, while optical paths offload large flows, inter-rack bulk transfers, or dedicated accelerator-to-accelerator channels. Helios exemplifies this hybrid logic by combining electrical packet switching with optical circuit switching for modular data centers. Modern variants may use co-packaged optics at the top-of-rack or switch level, with optical cross-connects for spine or super-spine layers. The architectural challenge is to design a topology that preserves bisection bandwidth without excessive optical port count. Fat-tree, dragonfly, and Clos topologies can be adapted, but each imposes different demands on optical transceiver count, cabling, and switching

granularity. A dragonfly-like optical fabric may reduce diameter, while a Clos-like fabric may simplify modular expansion [3], [10], [11].

Control and management planes determine whether these architectures deliver hardware efficiency. Optical paths require path computation, wavelength assignment, power equalization, and fault localization. If reconfiguration is centralized and slow, the fabric cannot respond to bursty AI traffic. If it is fully distributed, it may oscillate or conflict. A practical control plane may combine centralized optimization for long-timescale planning with distributed or hardware-accelerated scheduling for microsecond decisions. Telemetry from optical transceivers can provide per-wavelength power, bit error rate, and temperature data. This telemetry can be used for predictive maintenance, adaptive modulation, and thermal-aware routing. Without such instrumentation, optical fabrics become opaque, and operators may overprovision or revert to electrical fallback paths [12], [14], [17].

5. Trade-offs in Bandwidth, Latency, Energy, and Cost

The central trade-off in optical AI networks is between bandwidth density and energy efficiency. Higher-order modulation can increase per-wavelength capacity but requires more linear drivers, higher optical signal-to-noise ratio, and more complex digital signal processing. Dense wavelength-division multiplexing increases fiber capacity but demands stable lasers, precise filters, and thermal control. Co-packaged optics reduce electrical trace loss but concentrate heat near switch ASICs. Pluggable optics simplify replacement but consume more power at the front panel. There is no single optimum because the relative cost of power, cooling, floor space, and downtime varies by facility and region. Hardware-efficient design must therefore be contextual rather than universal [4], [6], [15].

Latency has multiple components: serialization delay, propagation delay, electro-optical conversion, switching delay, and control-plane delay. Optical fiber has lower loss than copper but light travels at roughly two-thirds the speed of light in vacuum, so propagation delay is not negligible over large data centers. Optical circuit reconfiguration can dominate latency if it takes milliseconds. Frequency-referenced multiplexing may reduce tuning and synchronization delays by providing stable, guaranteed channels, which can improve tail latency for collective operations [13]. Nevertheless, the end-to-end latency also depends on the electrical packet switch, network interface, and software stack. An optical link that saves nanoseconds at the physical layer may be irrelevant if the collective communication library introduces microseconds of jitter. Thus, latency optimization must be end-to-end and workload-aware [9], [13], [16].

Cost is often the decisive constraint. Optical transceivers, lasers, and switches have higher component costs than electrical equivalents at low volume, though silicon photonics promises economies of scale. Packaging and testing can account for a large fraction of photonic module cost. Co-packaged optics may reduce system power but increase replacement cost because a failed optical engine can affect an entire switch. Operators must weigh capital expenditure against operational expenditure, including cooling, spares, and technician time. A fabric that is highly efficient in energy per bit but difficult to repair may have a higher total cost of ownership. Hardware efficiency therefore includes maintainability and supply-chain resilience, not only raw performance [14], [15], [17].

Reliability and robustness are also part of the trade-off. Lasers degrade, modulators drift with temperature, and connectors accumulate contamination. Optical fabrics may require redundant paths, automatic protection switching, and graceful degradation to electrical

fallback. Redundancy increases cost and complexity, but it is necessary for AI training jobs that run for days or weeks. A single link failure can stall a collective operation and waste expensive accelerator time. Consequently, fault tolerance should be designed into the optical architecture from the beginning, rather than added as an afterthought. This favors modular designs with redundant light sources, monitor photodiodes, and reconfigurable paths [12], [14], [18].

6. Governance, Deployment, and Operational Robustness

Technical efficiency does not guarantee successful deployment. Governance structures shape procurement, standardization, and operational practice. Data center operators must decide whether to adopt proprietary optical solutions or wait for interoperable standards. Proprietary co-packaged optics may offer better performance but create vendor lock-in and complicate multi-vendor sourcing. Standards from IEEE, ITU, and optical networking alliances can reduce integration risk, but standards often lag behind rapid AI hardware cycles. A governance strategy should balance early adoption with long-term flexibility, perhaps through modular interfaces and multi-source agreements [1], [11].

Operational robustness requires visibility. Optical networks can fail silently through gradual power degradation or wavelength drift. Telemetry at the transceiver, switch, and link level can detect anomalies before they cause outages. Machine learning can be used for fault prediction, but it requires labeled data and careful validation. Operators need clear escalation paths, spares management, and training programs for photonic maintenance. In many organizations, optical expertise is concentrated in a small team, creating a single point of organizational failure. Governance should therefore include knowledge distribution, documentation, and simulation environments for safe reconfiguration [12], [14], [17].

Security and supply-chain concerns add further dimensions. Optical fibers are difficult to tap without detection, but optical switches and transceivers are complex electronic-photonic systems with firmware and management interfaces that can be attacked. Supply chains for lasers, indium phosphide, and advanced packaging are geographically concentrated, creating geopolitical risk. A resilient architecture may require dual sourcing, domestic manufacturing incentives, or strategic stockpiles. These are not purely technical decisions; they involve trade policy, industrial strategy, and risk management. Hardware-efficient optical AI infrastructure must therefore be understood as a socio-technical system [1], [14].

7. Sustainability, Fairness, and Policy Implications

Sustainability is a growing constraint on AI data centers. Energy consumption for computation and cooling is visible, but embodied carbon in servers, switches, and photonic modules is also significant. Optical interconnects may reduce operational energy by lowering signaling power, but they require additional manufacturing processes, rare materials, and precision packaging. Lifecycle assessment should compare electrical and optical architectures across manufacturing, deployment, operation, and disposal. Liquid cooling and waste heat recovery can improve efficiency, but they interact with photonic packaging and reliability. A sustainable design must consider water use, refrigerant leakage, and e-waste alongside electricity [2], [14], [18].

Fairness and equity are also implicated. Advanced AI data centers are concentrated in regions with cheap power, favorable tax policies, and robust fiber connectivity. This concentration can exclude smaller institutions, developing countries, and public-interest researchers from participating in frontier AI. Optical hardware efficiency could lower the cost of

communication, but it may also raise the minimum scale for competitive infrastructure. Policy responses might include shared research facilities, open standards, tiered access, and transparency about energy and water use. Procurement rules can favor modular, repairable, and interoperable designs that reduce lock-in and extend equipment lifetimes [1], [2], [18].

Policy implications extend to network neutrality and interconnection. If AI training clusters rely on dedicated optical paths across campuses or metro regions, regulators may need to clarify access, pricing, and competition rules. Spectrum and physical infrastructure sharing can lower barriers to entry. At the same time, overregulation could slow innovation in a rapidly evolving field. A balanced approach would encourage transparency, interoperability, and environmental reporting while allowing experimentation in architecture and business models. The goal is not to prescribe a single optical technology but to create governance conditions in which hardware-efficient and socially beneficial designs can emerge [2], [14], [18].

8. Future Directions and Research Agenda

Future research should pursue co-design across AI models, communication libraries, network controllers, and photonic hardware. Training algorithms could be adapted to network topology, for example by scheduling communication phases to match optical circuit availability. Communication libraries could expose flow predictability to the network, enabling proactive path setup. Network controllers could use reinforcement learning or optimization to allocate wavelengths and circuits while respecting latency and fairness constraints. These software advances must be validated on realistic testbeds with optical switches, co-packaged optics, and heterogeneous accelerators [3], [12], [13].

Another direction is the integration of optics with chiplets and advanced packaging. Monolithic or heterogeneous integration of photonics with accelerator dies could reduce electrical interface power and increase bandwidth density. Optical memory fabrics might allow disaggregated memory pools with high throughput. However, such architectures raise thermal, testing, and yield challenges. Research should quantify the energy and reliability trade-offs of co-packaged versus pluggable optics at different scales. It should also develop standards for optical interfaces, management, and telemetry so that multi-vendor fabrics can operate reliably [8], [9], [15], [18].

Finally, research should examine governance and sustainability as design variables. Lifecycle assessment methods for photonic components need improvement. Fair access to AI infrastructure requires empirical study of cost structures, regional disparities, and policy interventions. Robustness requires stress testing under correlated failures, adversarial conditions, and supply-chain disruptions. Hardware-efficient optical AI data centers will not be achieved by device breakthroughs alone. They will require integrated research programs that connect photonics, computer architecture, networking, economics, and public policy [1], [2], [13], [14].

9. Conclusion

Hardware-efficient optical communication architectures offer a credible path toward scaling AI data center networks beyond the limits of electrical interconnects. Optical links can provide higher bandwidth density, lower loss over distance, and wavelength parallelism, while silicon photonics and co-packaged optics promise improved energy efficiency. However, efficiency is not inherent to optics. It emerges from the co-design of transceivers, switches, packaging, control planes, telemetry, and deployment practices. Pure optical circuit

switching, optical packet switching, and hybrid electrical-optical fabrics each have distinct trade-offs in latency, granularity, cost, and reliability. Workload-aware architectures that exploit the synchronized and bursty nature of AI communication are particularly promising, especially when supported by stable frequency references and guaranteed-bandwidth channels [13].

The analysis also shows that hardware efficiency is embedded in broader socio-technical systems. Governance shapes standardization, procurement, and operational resilience. Sustainability requires lifecycle thinking about energy, materials, and e-waste. Fairness and policy determine who can access and benefit from advanced AI infrastructure. Future progress will depend on interdisciplinary research that treats photonic devices, network architecture, software control, and institutional design as mutually constitutive. If pursued with appropriate governance and sustainability safeguards, hardware-efficient optical fabrics can support the next generation of AI while reducing the resource intensity and fragility of current data center networks.

References

1. Cisco. (2023). Cisco annual internet report (2018–2023) white paper. Cisco Systems.
2. Shalf, J. (2020). The future of computing beyond Moore's Law. *Philosophical Transactions of the Royal Society A*, 378(2166), 20190061. <https://doi.org/10.1098/rsta.2019.0061>
3. Kachris, C., & Tomkos, I. (2012). A survey on optical interconnects for data centers. *IEEE Communications Surveys & Tutorials*, 14(4), 1021–1036. <https://doi.org/10.1109/SURV.2011.122111.00069>
4. Miller, D. A. B. (2009). Device requirements for optical interconnects to silicon chips. *Proceedings of the IEEE*, 97(7), 1166–1185. <https://doi.org/10.1109/JPROC.2009.2014298>
5. Benner, A. F., Ignatowski, M., Kash, J. A., Kuchta, D. M., & Ritter, M. B. (2005). Exploitation of optical interconnects in future server architectures. *IBM Journal of Research and Development*, 49(4/5), 755–775. <https://doi.org/10.1147/rd.494.0755>
6. Asghari, M., & Krishnamoorthy, A. V. (2011). Silicon photonics: Energy-efficient communication. *Nature Photonics*, 5(5), 268–270. <https://doi.org/10.1038/nphoton.2011.68>
7. Soref, R. (2006). The past, present, and future of silicon photonics. *IEEE Journal of Selected Topics in Quantum Electronics*, 12(6), 1678–1687. <https://doi.org/10.1109/JSTQE.2006.883151>
8. Sun, C., Wade, M. T., Lee, Y., Orcutt, J. S., Alloatti, L., Georgas, M. S., ... & Stojanović, V. M. (2015). Single-chip microprocessor that communicates directly using light. *Nature*, 528(7583), 534–538. <https://doi.org/10.1038/nature16454>
9. Atabaki, A. H., Moazeni, S., Pavanello, F., Gevorgyan, H., Notaros, J., Alloatti, L., ... & Ram, R. J. (2018). Integrating photonics with silicon nanoelectronics for the next generation of systems on a chip. *Nature*, 556(7701), 349–354. <https://doi.org/10.1038/s41586-018-0028-z>
10. Farrington, N., Porter, G., Radhakrishnan, S., Bazzaz, H. H., Subramanya, V., Fainman, Y., Papen, G., & Vahdat, A. (2010). Helios: A hybrid electrical/optical switch

architecture for modular data centers. *ACM SIGCOMM Computer Communication Review*, 40(4), 339–350. <https://doi.org/10.1145/1851182.1851223>

11. Bitar, N., Gringeri, S., & Xia, T. J. (2013). Technologies and protocols for data center and cloud networking. *IEEE Communications Magazine*, 51(9), 24–31. <https://doi.org/10.1109/MCOM.2013.6588645>
12. Cheng, Q., Rumley, S., Bahadori, M., & Bergman, K. (2018). Photonic switching in high performance datacenters. *Optics Express*, 26(12), 16022–16043. <https://doi.org/10.1364/OE.26.016022>
13. Zhou, Z., Wei, J., Luo, Y., Clark, K. A., Siljekens, E., Deakin, C., ... & Liu, Z. (2023). Communications with guaranteed bandwidth and low latency using frequency-referenced multiplexing. *Nature Electronics*, 6(9), 694-702.
14. Rickman, A. (2014). The commercialization of silicon photonics. *Nature Photonics*, 8(8), 579–582. <https://doi.org/10.1038/nphoton.2014.175>
15. Thomson, D., Zilkie, A., Bowers, J. E., Komljenovic, T., Reed, G. T., Vivien, L., ... & Nedeljkovic, M. (2016). Roadmap on silicon photonics. *Journal of Optics*, 18(7), 073003. <https://doi.org/10.1088/2040-8978/18/7/073003>
16. Vlasov, Y. A. (2012). Silicon CMOS-integrated nano-photonics for computer and data communications beyond 100G. *IEEE Communications Magazine*, 50(2), S67–S72. <https://doi.org/10.1109/MCOM.2012.6146487>
17. Doerr, C. R. (2015). Silicon photonic integration in telecommunications. *Frontiers in Physics*, 3, 37. <https://doi.org/10.3389/fphy.2015.00037>
18. Smit, M., van der Tol, J., & Hill, M. (2012). Moore's law in photonics. *Laser & Photonics Reviews*, 6(1), 1–13. <https://doi.org/10.1002/lpor.201100001>